University of Mumbai

1T04613

Winter 2025

EXAMINATION TIME TABLE

PROGRAMME - S.E. (VLSI Design & Technology) (Choice Based)

SEMESTER - III

Days and Dates	Time	Paper Code	Paper
Monday, 10 November, 2025	2:30 p.m. to 05:30 p.m.	31121	Engineering Mathematics-III
Wednesday, 12 November, 2025	2:30 p.m. to 05:30 p.m.	31122	Electronics Devices & Circuits I
Friday, 14 November, 2025	2:30 p.m. to 05:30 p.m.	31123	Digital Logic Circuits
Tuesday, 18 November, 2025	2:30 p.m. to 05:30 p.m.	31124	Electrical Networks Analysis & Synthesis
Thursday, 20 November, 2025	2:30 p.m. to 05:30 p.m.	31125	Electronic Instruments & Measurements

Important Note: •The candidates appearing for the examination should report 20 minutes before the start of examination.
- Mobile phones and other elctronic gazets are prohibited in the examination hall.
- Change if any, in the time table shall be communicated on the university web site.

Mumbai - 400 098
26th July, 2025.

Dr.Pooja Raundale
Director
Board of Examinations & Evaluation