Q.P. Code:00003964

[Time:2.30 Hrs] **[Marks:75]**

Please check whether you have got the right question paper.

N.B:
1. All questions are compulsory.
2. Figures to the right indicate full marks.
3. Students answering in the regional language should refer in case of doubt to the main text of the paper in English.

Q1 Attempt **any three** of the following: **[15]**

(a) What is analog signal? Explain frequency, amplitude with respect to analog signal.

(b) Show the following decimal to binary number system conversions

i)25.45 ii) 134

(c) Show conversion of the 10101100 BCD code into Gray code and also in Excess-3 code.

(d) Explain the difference between analog signal and digital signal.

(e) Solve the following number conversions.

i) $(17E.F6)_{16} = (?)_2$ ii) $(110010100011.10100101)_2 = (?)_{16}$

(f) Solve the following number conversions.

i) $(125.50)_{10} = (?)_2$ ii) $(110001)_2 = (?)_{10}$

Q2 Attempt **any three** of the following: **[15]**

(a) For the logic expression Y=AB'+A'B. Obtain the truth table, name the gate and operation performed and symbol for it also explain this using AND, OR, NOT gates.

(b) Prove the given Boolean expression using Boolean laws and draw the circuit for it using NAND gates only. A.B+A'B+A'B'=A'+B

(c) State and prove De-Morgan's theorem and realize it using basic gates.

(d) What is meant by universal logic gate? Construct Ex-OR gate using NAND gate and using NOR gate

(e) F (A, B, C, D) =∑m (0,1,2,5,13,15). Simplicity using k-map and find minimized Boolean expression.

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(f) What is meant by don't care conditions? Explain how they are used in simplifying an expression using a k-map. Use the following example-

F (A, B, C, D) = ∑m (1,4,8,12,13,15) + d (3,14)

Q3 Attempt **any three** of the following: **[15]**

(a) Construct a 4-bit full adder using 3 full adders.

(b) With the help of K-maps construct a two-bit half adder and describe it working.

(c) Explain with example code conversion from binary to gray.

(d) Design a combinational circuit for the following description. The circuit has 4 inputs and 2 outputs. One of the outputs is true if the major inputs are true. The other output is true if there is a tie between 4 inputs.

(e) Construct 1-bit comparator using truth table.

(f) Explain the working of a BCD subtractor.

Q4 Attempt **any three** of the following: **[15]**

(a) Explain clocked SR-flip flop in detail with the help of logic diagram.

(b) Explain how JK flip flop can be used to form D flip flop.

(c) Draw a neat circuit diagram and explain the working of 1:4 Demultiplexer.

(d) With the help of suitable diagram explain the working of 2 to 4 decoder.

(e) Construct 8:1 Multiplexer using two 4:1 multiplexer.

(f) Construct the following using 8:1 multiplexer.

i) $F(A,B,C,D) = \Sigma m(2,4,5,7,10,14)$
ii) $F(A,B,C,D) = \Sigma m(1,5,6,9,10)$

Q5 Attempt **any three** of the following: **[15]**

(a) Design 2-bit synchronous down counter

(b) Compare between counters and shift registers

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(c) With the help of suitable diagrams explain 3-bit asynchronous up-counter

(d) With the help of suitable diagrams explain Ring Counter.

(e) Explain the architecture of SISO registers.

(f) Design and explain modulo 5 synchronous counters.