

# University of Mumbai



**1T04613**

Winter 2024

## EXAMINATION TIME TABLE

### PROGRAMME - S.E. (VLSI Design & Technology) (Choice Based)

#### SEMESTER - III

Days and Dates	Time	Paper Code	Paper
Tuesday, 12 November, 2024	2:30 p.m. to 05:30 p.m.	31121	Engineering Mathematics-III
Thursday, 14 November, 2024	2:30 p.m. to 05:30 p.m.	31122	Electronics Devices & Circuits I
Tuesday, 19 November, 2024	2:30 p.m. to 05:30 p.m.	31123	Digital Logic Circuits
Thursday, 21 November, 2024	2:30 p.m. to 05:30 p.m.	31124	Electrical Networks Analysis & Synthesis
Monday, 25 November, 2024	2:30 p.m. to 05:30 p.m.	31125	Electronic Instruments & Measurements

Important Note: •The candidates appearing for the examination should report 20 minutes before the start of examination.

- Mobile phones and other electronic gadgets are prohibited in the examination hall.
- Change if any, in the time table shall be communicated on the university web site.

Mumbai - 400 098  
4<sup>th</sup> November, 2024.

*y.p. Raundale*

Dr. Pooja Raundale  
Director  
Board of Examinations & Evaluation