AC –20/5/2025
Item No. – 6.57 (N) 1

As Per NEP 2020

University of Mumbai

Syllabus for Minor Vertical 2		
Faculty of Engineering		
Board of Studies in Computer Engineering		
Second Year Programme in Minor Computer Engineering		
Semester	**IV**	
Title of Paper (Theory)	**Sem.**	**Total Credits 4**
Computer Organization & Architecture	**IV**	**3**
Title of Paper (Lab)		**Credits**
Computer Organization & Architecture Lab	**IV**	**1**
From the Academic Year		**2025-26**

Sem. - IV

Course Code	Course Name	Teaching Scheme (Contact Hours)			Credits Assigned			
		Theory	Pract.	Tut.	Theory	Pract.	Tut.	Total
2454211	Computer Organization & Architecture	3	-	-	3	-	-	3

Course Code	Course Name	Evaluation Scheme (Theory)					Term work	Pract / Oral	Total
		Internal Assessment			End Sem Exam	Exam Duration (in Hrs)			
		Test 1	Test 2	Avg.					
2454211	Computer Organization & Architecture	20	20	40	60	2	-	-	100

Pre-requisite.	Fundamental of Mathematics
Course Objective: To study the fundamentals of number system and arithmetic operations. To equip students with the foundational knowledge of computer organization and architecture, fostering an understanding of how hardware and software components collaborate to execute tasks, and preparing them to design and optimize computing systems for real-world applications.	
Course Outcomes (CO): *At the End of the course students will be able to*	
CO.1	Conceptualize basic computer structure with its models.
CO.2	Design algorithms to solve ALU operations
CO.3	Comprehend processor organization with various control signal design methods of CPU with comparative analysis.
CO.4	Design memory systems with analysis of mapping techniques for cache memory.
CO.5	Explore different types of I/O buses, examine data transfer methods, and assess arbitration techniques for optimized system performance.
CO.6	Analyze different parallel organizations that includes pipelined and parallel processors

Detailed Syllabus:

Module No.	Unit No.	Topics	Hrs	CO Mapping
1	Title	**Computer Fundamentals**	4	1
	1.1	Number Systems: Binary. Octal and Hexadecimals. Binary Number representation: Sign Magnitude, 1's and 2's Compliment representation. Logic Gates: AND, OR, NOT, NAND, NOR, EX-OR Basic Organization of Computer, Von Neumann model.		
2	Title	**ALU Operations**	7	2
	2.1	ALU Operation: Addition and Subtraction on Binary, Octal, Hexadecimal number.		
	2.2	Booth's Algorithms, Restoring and Non restoring division algorithm.		
	2.3	IEEE 754 Floating point representation and conversation.		
3	Title	**Processor Organization and Control Unit Design**	8	3
	3.1	Architecture of 8086 processor, Register Organization, Instruction formats, instruction cycle, addressing modes.		
	3.2	Control Unit: Instruction interpretation and sequencing, Micro-programmed and hardwired control unit design methods. Microinstruction sequencing and execution, Micro programs.		

	3.3	RISC and CISC: Introduction to RISC and CISC architectures and design issues.		
4	**Title**	**Memory Systems Organization**	**8**	4
	4.1	Introduction to Memory and Memory parameters. Classifications of primary and secondary memories. Types of RAM and ROM, Memory hierarchy and characteristics, Virtual Memory: Segmentation and Paging		
	4.2	Cache memory: Concept, hierarchy (L1, L2, L3), mapping techniques. Cache Coherency and technique to resolve it. Interleaved and Associative memory.		
	Self-Study	Case study of Pentium Processor Cache Memory Model (MESI Protocol)		
5	**Title**	**I/O Organization**	**4**	5
	5.1	Buses: Types of Buses, Bus Arbitration, Bus standards and its comparative study		
	5.2	I/O Interface, I/O channels, I/O modules and IO processor, Types of data transfer techniques: Programmed I/O, Interrupt driven I/O and DMA.		
6	**Title**	**Parallel Processing**	**8**	6
	6.1	Advanced Processor Models(80386DX): Real Model, Protected Model, Virtual Model		
	6.2	Pipelined Architecture: Pipeline Stages, Superscalar architecture Pipeline Hazards, Mitigation of Hazards with branch prediction and data forwarding techniques, Amdahl's Law		
	6.3	Introduction to parallel processing concepts, Flynn's classifications,		
	Self-Study	Superscalar Architecture: Case study of Pentium processor and GPGPU architecture.		

Text Books:

Sr. No	Title	Edition	Authors	Publisher	Year
1	Modern Digital Electronics	4th	R P Jain	Tata McGraw-Hill	2009
2	Computer Organization	5th	Carl Hamacher, Zvonko Vranesic and Safwat Zaky	Tata McGraw-Hill	2002
3	Computer Architecture and Organization	3rd	John P. Hayes	Tata McGraw-Hill	2012
4	Computer Organization and Architecture: Designing for Performance	8th	William Stallings	Pearson	2010
5	Microprocessors and Interfacing	3rd	Douglas V Hall	Tata McGraw-Hill	2017
6	The 80386, 80486, and Pentium Microprocessor: Hardware, Software, and Interfacing	3rd	Walter Triebel	Pearson	1997
7	Pentium Pro Processor System Architecture	3rd	Tom Shanely	Addison Wesley	1996

Reference Books

Sr. No	Title	Edition	Authors	Publisher	Year
1	Structured Computer Organization	6th	Andrew S. Tanenbaum	Pearson	2012
2	Computer Architecture and Organization: Design Principles and Applications	2nd	B. Govindarajulu	McGraw Hill	2017
3	Advance Computer Architecture: Parallelism, Scalability, Programmability	3rd	Kai Hwang	Tata-McGraw Hill	2017

4	Microcomputer System The 8086/8088 family	2nd	Liu and Gibson	Pearson	2015
5	Programmer's reference Manual for IBM Personal Computers	1st	Steven Armburst	Tata-McGraw Hill	

Online References:

Sr. No.	Website Name
1.	https://www.classcentral.com/course/swayam-computer-organization-and-architecture-a-pedagogical-aspect-9824
2.	https://nptel.ac.in/courses/106/103/106103068/
3.	https://www.coursera.org/learn/comparch
4	https://www.edx.org/learn/computer-architecture

Assessment:

Internal Assessment (IA) for 20 marks:

- IA will consist of Two Compulsory Internal Assessment Tests. Approximately 40% to 50% of syllabus content must be covered in First IA Test and remaining 40% to 50% of syllabus content must be covered in Second IA Test

- **Question paper format**

  - Question Paper will comprise of a total of **six questions each carrying 20 marksQ.1** will be **compulsory** and should **cover maximum contents of the syllabus**

  - **Remaining questions** will be **mixed in nature** (part (a) and part (b) of each question must be from different modules. For example, if Q.2 has part (a) from Module 3 then part (b) must be from any other Module randomly selected from all the modules)

  - A total of **Three questions** need to be answered

Course Code	Course Name	Teaching Scheme (Contact Hours)			Credits Assigned			
		Theory	Pract.	Tut.	Theory	Pract.	Tut.	Total
2454212	Computer Organization & Architecture Lab	-	2	-	-	1	-	1

Course Code	Course Name	Examination Scheme						
		Theory Marks				Term Work	Practical/ Oral	Total
		Internal assessment			End Sem. Exam			
		Test	Test 2	Avg. of 2 Tests				
2454212	Computer Organization & Architecture Lab	--	--	--	--	25	25	50

Prerequisite: C/C++ Programming Language.	
Lab Objectives:	
1	To study and learn assembler and using its utilities.(MASM)
2	To write assembly language programs.
3	To perform various ALU operations using assembly language programs.
4	To enable and use graphical mode in assembly language programs.
5	To implement arithmetics operations using algorithms.
6	To implement cache memory mapping techniques.

Lab Outcomes: At the end of the course, student will be able to	
1	To install the MASM.
2	Write assembly language programs.
3	Utilised various utility of INT 21H interrupts.
4	Utilised various utility of INT 10H interrupts.
5	Simulate various algorithms.
6	Simulate varus cache memory mapping techniques.

Sr. No	Title of the Experiment	LO
1	Installation and configure: DOS, MASM, Debug and X86 Mode	1
2	Implementation of various ALU operations (ADD, SUB, MUL, DIV, AND, OR, XOR, NOT) through assembly language programming for 8086 using MASM and Debug.	2
3	Implementation of number conversion (HEX to BCD, ASCII to BCD, BCD to ASCII) using MASM.	2
4	Implementation of two 8-bit BCD addition with accepting input from keyboard and displaying output on monitor using INT 21H interrupts.	3
5	Implement various String Operations in 8086 through the utilities provided by DOS and BIOS interrupts (MASM)	2
6	Block Transfer and Block Exchange using Index Registers.	2
7	Drawing basic shapes like rectangle, triangle, etc. using BIOS services [Use C/MASM]	4
8	Design Password Detection Application using BIOS and DOS interrupts along with 8086 instructions.	2
9	Implement file operations [DOS Interrupts in C/MASM]	2
10	Implement I/O interfacing using inbuilt speakers of IBM PC	2

11	Implementation of cursor activity like hiding cursor and changing it to box size using INT 10H interrupts.	4
12	Implement Booth's Multiplication Algorithm	5
13	Implement Division Algorithm (Non-Restoring and/or Restoring)	5
14	Implementation of Mapping techniques of Cache memory	6
15	Displaying 8086 processor's Flag register content on monitor.	2
16	Designing 4X4 memory using 1X1 memory chips. Use COA virtual lab by IIT Kharagpur.	

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2.	https://nptel.ac.in/courses/106/103/106103068/
3.	https://www.coursera.org/learn/comparch
4	https://www.edx.org/learn/computer-architecture
5	http://cse10-iitkgp.virtual-labs.ac.in/

Sr No	List of Assignments	Hrs
01	Number conversion from one base to another and addition and subtraction on converted numbers.	
02	Numerical on Booth's Algorithm and on Restoring and Non restoring algorithm.	

	IEEE 754 conversion.	
03	Numerical on Cache memory mapping. Cache coherency and resolution methods.	
04	Different techniques for designing control unit of computer.	
05	Different data transfer techniques and bus arbitration.	
06	Pipeline and pipeline hazards.	
07	Flynn's classification scheme.	
08	Memory interleaving and associative memory.	

Assessment:

Term Work: Term Work shall consist of at least 10 to 12 practical's based on the above list. Also, Term work Journal must include at least 2 assignments.

Term Work Marks: 25 Marks (Total marks) = 15 Marks (Experiment) + 5 Marks (Assignments) + 5 Marks (Attendance)

Practical& Oral Exam: An Oral & Practical exam will be held based on the theory and practical syllabus.