

# University of Mumbai

**1T04613**

Summer 2025

## EXAMINATION TIME TABLE

### PROGRAMME - S.E. (VLSI Design & Technology) (Choice Based)

#### SEMESTER - III

| Days and Dates          | Time                    | Paper Code | Paper                                    |
|-------------------------|-------------------------|------------|------------------------------------------|
| Monday, 2 June, 2025    | 2:30 p.m. to 05:30 p.m. | 31121      | Engineering Mathematics-III              |
| Wednesday, 4 June, 2025 | 2:30 p.m. to 05:30 p.m. | 31122      | Electronics Devices & Circuits I         |
| Friday, 6 June, 2025    | 2:30 p.m. to 05:30 p.m. | 31123      | Digital Logic Circuits                   |
| Tuesday, 10 June, 2025  | 2:30 p.m. to 05:30 p.m. | 31124      | Electrical Networks Analysis & Synthesis |
| Thursday, 12 June, 2025 | 2:30 p.m. to 05:30 p.m. | 31125      | Electronic Instruments & Measurements    |

Important Note: •The candidates appearing for the examination should report 20 minutes before the start of examination.

- Mobile phones and other electronic gadgets are prohibited in the examination hall.
- Change if any, in the time table shall be communicated on the university web site.

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28<sup>th</sup> April, 2025.

Dr. Pooja Raundale

Director

Board of Examinations & Evaluation