

University of Mumbai



No. AAMS_UGS/ICC/2022-23/ 182

CIRCULAR:-

Attention of the Principals of the Affiliated Colleges and Directors of the Recognized Institutions in Faculty of Science & Technology is invited to the syllabus uploaded by Academic Authority Meetings & Services which was accepted by the Academic Council at its meeting held on 14th July, 2016 vide item No. 4.22 relating to the revised syllabus as per Choice Based Credit and Grading System for M.E. (Electronics Engineering).

You are hereby informed that the recommendations made by the Ad-hoc Board of Studies in **Electronics Engineering** at its meeting held on 22nd June, 2022 and subsequently passed in the Faculty and then by the Board of Deans at its meeting held on 5th July, 2022 vide item No. 6.60 (R) have been accepted by the Academic Council at its meeting held on 11th July, 2022 vide item No. 6.60 (R) and that in accordance therewith, the revised syllabus of **M.E. (Electronics Engineering) (CBCS) (Sem.- I to IV) (REV - 2022 Scheme)**, has been brought into force with effect from the academic year 2022-23. (The circular is available on the University's website www.mu.ac.in).

MUMBAI - 400 032
19th November, 2022
To


(Prof. Sunil Bhirud)
I/c Registrar

The Principals of the Affiliated Colleges and Directors of the Recognized Institutions in Faculty of Science & Technology.

A.C/6.60 (R)/11/07/2022

Copy forwarded with Compliments for information to:-

- 1) The Dean, Faculty of Science & Technology,
- 2) The Chairman, Board of Studies in Electronics Engineering,
- 3) The Director, Board of Examinations and Evaluation,
- 4) The Director, Board of Students Development,
- 5) The Director, Department of Information & Communication Technology,
- 6) The Co-ordinator, MKCL.

Copy to :-

- 1. The Deputy Registrar, Academic Authorities Meetings and Services (AAMS),**
- 2. The Deputy Registrar, College Affiliations & Development Department (CAD),**
- 3. The Deputy Registrar, (Admissions, Enrolment, Eligibility and Migration Department (AEM),**
- 4. The Deputy Registrar, Research Administration & Promotion Cell (RAPC),**
- 5. The Deputy Registrar, Executive Authorities Section (EA),**
- 6. The Deputy Registrar, PRO, Fort, (Publication Section),**
- 7. The Deputy Registrar, (Special Cell),**
- 8. The Deputy Registrar, Fort/ Vidyanagari Administration Department (FAD) (VAD), Record Section,**
- 9. The Director, Institute of Distance and Open Learning (IDOL Admin), Vidyanagari,**

They are requested to treat this as action taken report on the concerned resolution adopted by the Academic Council referred to in the above circular and that on separate Action Taken Report will be sent in this connection.

- 1. P.A to Hon'ble Vice-Chancellor,**
- 2. P.A Pro-Vice-Chancellor,**
- 3. P.A to Registrar,**
- 4. All Deans of all Faculties,**
- 5. P.A to Finance & Account Officers, (F.& A.O),**
- 6. P.A to Director, Board of Examinations and Evaluation,**
- 7. P.A to Director, Innovation, Incubation and Linkages,**
- 8. P.A to Director, Board of Lifelong Learning and Extension (BLLE),**
- 9. The Director, Dept. of Information and Communication Technology (DICT) (CCF & UCC), Vidyanagari,**
- 10. The Director of Board of Student Development,**
- 11. The Director, Department of Students Welfare (DSD),**
- 12. All Deputy Registrar, Examination House,**
- 13. The Deputy Registrars, Finance & Accounts Section,**
- 14. The Assistant Registrar, Administrative sub-Campus Thane,**
- 15. The Assistant Registrar, School of Engg. & Applied Sciences, Kalyan,**
- 16. The Assistant Registrar, Ratnagiri sub-centre, Ratnagiri,**
- 17. The Assistant Registrar, Constituent Colleges Unit,**
- 18. BUCTU,**
- 19. The Receptionist,**
- 20. The Telephone Operator,**
- 21. The Secretary MUASA**

for information.

University of Mumbai



**Revised Syllabus for
M.E. (Electronics Engineering)
(Sem. - I to IV)
(Choice Based Credit System)**

(With effect from the academic year 2022-23)

University of Mumbai



Syllabus for Approval

O: _____	Title of Course	M.E. (Electronics Engineering)
O: <u>5134 Eligibility</u>		Passed B.E./ B.Tech (Electronics Engg.); B.E./ B.Tech (Electronics and Telecommunication Engg.); B.E. (Electrical and Electronics Engg); B.E. (Electronics and Computer Science)
R: _____	Passing Marks	45%
No. of years/Semesters:		2 Years / 4 Semester
Level:		P.G. / U.G./ Diploma / Certificate
Pattern:		Yearly / Semester
Status:		New / Revised 2019 'C'
To be implemented from Academic Year:		With effect from Academic Year : 2022-23

Dr. R. N. Awale
Chairman
of Ad-hoc Board of
Studies in Electronics
Engineering

Dr. Suresh K. Ukarande
Associate Dean,
Faculty of Science and
Technology

Dr Anuradha Majumdar
Dean,
Faculty of Science and
Technology

Preamble

To meet the challenge of ensuring excellence in engineering education, the issue of quality needs to be addressed, debated and taken forward in a systematic manner. Accreditation is the principal means of quality assurance in higher education. The major emphasis of accreditation process is to measure the outcomes of the program that is being accredited. In line with this Faculty of Science and Technology (in particular Engineering) of University of Mumbai has taken a lead in incorporating philosophy of outcome based education in the process of curriculum development.

Faculty resolved that course objectives and course outcomes are to be clearly defined for each course, so that all faculty members in affiliated institutes understand the depth and approach of course to be taught, which will enhance learner's learning process. Choice based Credit and grading system enables a much-required shift in focus from teacher-centric to learner-centric education since

the workload estimated is based on the investment of time in learning and not in teaching. It also focuses on continuous evaluation which will enhance the quality of education. Credit assignment for courses is based on 15 weeks teaching learning process, however content of courses is to be taught in 12-13 weeks and remaining 2-3 weeks to be utilized for revision, guest lectures, coverage of content beyond syllabus etc. There was a concern that the earlier revised curriculum more focused on providing information and knowledge across various domains of the said program, which led to heavily loading of students in terms of direct contact hours. In this regard, faculty of science and technology resolved that to minimize the burden of contact hours, total credits of entire program will be of 170, where focus is not only on providing knowledge but also on building skills, attitude and self-learning. Therefore in the present curriculum skill based laboratories and mini projects are made mandatory across all disciplines of engineering in second and third year of programs, which will definitely facilitate self-learning of students. The overall credits and approach of curriculum proposed in the present revision is in line with AICTE model curriculum.

The present curriculum will be implemented for Second Year of Engineering from the academic year 2020-21. Subsequently this will be carried forward for Third Year and Final Year Engineering in the academic years 2021-22, 2022-23, respectively.

Dr.S. K. Ukarande
Associate Dean
Faculty of Science and Technology
University of Mumbai

Dr. Anuradha Muzumdar
Dean
Faculty of Science and Technology
University of Mumbai

Incorporation and implementation of Online Contents from NPTEL/Swayam Platform

The curriculum revision is mainly focused on knowledge component, skill based activities and project based activities. Self-

learning opportunities are provided to learners. In the revision process this time in particular Revised syllabus of „C „ scheme wherever possible additional resource links of platforms such as NPTEL, Swayam are appropriately provided. In an earlier revision of curriculum in the year 2012 and 2016 in Revised scheme „A' and „B' respectively, efforts were made to use online contents more appropriately as additional learning materials to enhance learning of students.

In the current revision based on the recommendation of AICTE model curriculum overall credits are reduced to 171, to provide opportunity of self-learning to learner. Learners are now getting sufficient time for self-

learning either through online courses or additional projects for enhancing their knowledge and skill sets.

The Principals/ HoD's/ Faculties of all the institute are required to motivate and encourage learners to use additional online resources available on platforms such as NPTEL/ Swayam. Learners can be advised to take up online courses, on successful completion they are required to submit certification for the same. This will definitely help learners to facilitate their enhanced learning based on their interest.

Dr.S. K. Ukarande
Associate Dean
Faculty of Science and Technology
University of Mumbai

Dr Anuradha Muzumdar
Dean
Faculty of Science and Technology
University of Mumbai

Preface

Technical education in the country is undergoing a paradigm shift in current days. Think tank at national level are deliberating on the issues, which are of utmost importance and posed challenge to all the spheres of technical education. Eventually, impact of these developments was visible and as well adopted on bigger scale by almost all universities across the country. These are primarily an adoption of CBCS (Choice based Credit System) and OBE (Outcome based Education) with student centric and learning centric approach. Education sector

in the country, as well, facing critical challenges, such as, the quality of graduates, employability, basic skills, ability to take challenges, work ability in the fields, adoption to the situation, leadership qualities, communication skills and ethical behaviour. On other hand, the aspirants for admission to engineering programs are on decline over the years. An overall admission status across the country is almost 50%; posing threat with more than half the vacancies in various colleges and make their survival difficult. In light of these, an All India Council for Technical Education (AICTE), the national regulator, took initiatives and enforced certain policies for betterment, in timely manner. Few of them are highlighted here, these are design of model curriculum for all prevailing streams, mandatory induction program for new entrants, introduction of skill based and inter/cross discipline courses, mandatory industry internships, creation of digital contents, mandate for use of ICT in teaching learning, virtual laboratory and soon.

To keep the pace with these developments in Technical education, it is mandatory for the Institutes & Universities to adopt these initiatives in phased manner, either partially or in toto. Hence, the ongoing curriculum revision process has a crucial role to play. The BoS of Electronics Engineering under the faculty of Science & Technology, under the gamut of Mumbai University has initiated a step towards adoption of these initiatives. We, the members of Electronics Engineering Board of Studies of Mumbai University feel privileged to present the revised version of curriculum for Electronics Engineering program to be implemented from academic year 2020-21. Some of the highlights of the revision are;

- i. Curriculum has been framed with reduced credits and weekly contact hours, thereby providing free slots to the students to brainstorm, debate, explore and apply the engineering principles. The leisure provided through this revision shall favour to inculcate innovation and research attitude amongst the students.
- ii. New skill based courses have been incorporated in curriculum keeping in view AICTE model curriculum.
- iii. Skill based Lab courses have been introduced, which shall change the thought process and enhance the programming skills and logical thinking of the students
- iv. Mini-project with assigned credits shall provide an opportunity to work in a group, balancing the group dynamics, develop leadership qualities, facilitate decision making and enhance problem solving ability with focus towards socio-economic development of the country. In addition, it shall be direct application of theoretical knowledge in practice, thereby, nurture learner to become industry ready and enlighten students for Research, Innovation and Entrepreneurship thereby to nurture start-up ecosystem with better means.
- v. A usage of ICT through NPTEL/SWAYAM and other Digital initiatives of Govt. of India shall be encouraged, facilitating the students for self learning and achieve the Graduate Attribute (GA) specified by National Board of Accreditation (NBA) i.e. lifelong learning.

Thus, this revision of curriculum aimed at creating deep impact on the teaching learning methodology to be adopted by affiliated Institutes, thereby nurturing the student fraternity in multifaceted directions and create competent technical manpower with legitimate skills. In times to come, these graduates shall shoulder the responsibilities of proliferation of future technologies and support in a big way for 'Make in India' initiative, a reality. In the process,

BoS, Electronics Engineering got whole hearted support from all stakeholders including faculty, Heads of department of affiliating institutes, experts faculty who detailed out the course contents, alumni, industry experts and university official providing all procedural support time to time. We put on record their involvement and sincerely thank one and all for contribution and support extended for this noble cause.

Board of Studies in Electronics Engineering

Sr.No.	Name	Designation	Sr.No.	Name	Designation
1	Dr.R.N.Awale	Chairman	5	Dr.Rajani Mangala	Member
2	Dr.Jyothi Digge	Member	6	Dr.Vikas Gupta	Member
3	Dr.V.A.Vyawhare	Member	7	Dr.D. J.Pete	Member
4	Dr.Srija Unnikrishnan	Member	8	Dr.Vivek Agarwal	Member

Program Structure for MEElectronicsEngineering
UNIVERSITY OF MUMBAI
 (With Effect from 2022-2023)

Semester I

Course Code	Course Name	Teaching Scheme(Contact Hours)			Credits Assigned			
		Theory	Practical	Tutorial	Theory	Practical	Tutorial	Total
ELXC1011	Advanced Digital Communication	03	---	---	03	---	---	03
ELXC1012	Advanced VLSI Design	03	---	---	03	---	---	03
ELXC1013	Power Electronics System Design	03	---	---	03	---	---	03
ELXDLO101X	Department Level Optional Course-I	03	---	---	03	---	---	03
ILO101X	Institute Level Optional Course-I	03	---	---	03	---	---	03
ELXL1011	Laboratory-I Power Electronics System Design	---	02	---	---	01	---	01
ELXL1012	Laboratory-II Advanced VLSI Design	---	02	---	---	01	---	01
TOTAL		15	04	---	15	02	---	17

Course Code	CourseName	EXAMINATIONSCHEME–SEMESTER I							
		THEORY					MAXIMUMMARKS		
		INTERNALASSESSMENT(I A)			EndSemester Examination (Marks)	ExamDuration(Hours)			
		Test I	Test II	Avg.			Term Work	Practical / Oral	Total
ELXC1011	Advanced Digital Communication	20	20	20	80	03	---	---	100
ELXC1012	Advanced VLSI Design	20	20	20	80	03	---	---	100
ELXC1013	Power Electronics System Design	20	20	20	80	03	---	---	100
ELXDLO101X	Department Level Optional Course-I	20	20	20	80	03	---	---	100
ILO101X	Institute Level Optional Course-I	20	20	20	80	03	---	---	100
ELXL1011	Laboratory-I Power Electronics System Design	---	---	---	---	---	25	25	50
ELXL1012	Laboratory-II Advanced VLSI Design	---	---	---	---	---	25	25	50
TOTAL		100	100	100	400	---	50	50	600

Program Structure for MEElectronicsEngineering
UNIVERSITY OF MUMBAI
 (With Effect from 2022-2023)

Semester II

Course Code	Course Name	Teaching Scheme (Contact Hours)			Credits Assigned			
		Theory	Practical	Tutorial	Theory	Practical	Tutorial	Total
ELXC2021	Modern Industrial Internet Engineering	03	---	---	03	---	---	03
ELXC2022	Emerging Trends in SOC Design	03	---	---	03	---	---	03
ELXC2023	Advanced Digital Signal Processing	03	---	---	03	---	---	03
ELXDLO202X	Department Level Optional Course II	03	---	---	03	---	---	03
ILO202X	Institute Level Optional Course-II	03	---	---	03	---	---	03
ELXL2021	Laboratory- III Emerging Trends in SOC Design	---	02	---	---	01	---	01
ELXL2022	Laboratory- IV Advanced Digital Signal Processing (ADSP)	---	02	---	---	01	---	01
TOTAL		15	04	---	15	02	---	17

Course Code	CourseName	EXAMINATIONScheme–SemesterII							
		THEORY					MAXIMUMMARKS		
		INTERNAL ASSESSMENT (IA)			EndSemeste rExamination(Marks)	ExamDu ration(H ours)			
		Test I	Test II	Avg.			Term Work	Practical / Oral	Total
ELXC2021	Modern IndustrialInternetEn gineering	20	20	20	80	03	---	---	100
ELXC2022	Emerging TrendsinSOCDe sign	20	20	20	80	03	---	---	100
ELXC2023	Advanced DigitalSignalProc essing	20	20	20	80	03	---	---	100
ELXDLO202X	Department LevelOptionalCou rseII	20	20	20	80	03	---	---	100
ILO202X	Institute LevelOptionalCou rse-II	20	20	20	80	03	---	---	100
ELXL2021	Laboratory- IIIEmerging TrendsinSOCDe sign	---	---	---	---	---	25	25	50
ELXL2022	Laboratory- IVAdvanced DigitalSignalPro cessing (ADSP)	---	---	---	---	---	25	25	50
TOTAL		100	100	100	400	---	50	50	600

Course Code	DepartmentLevelOptional Course-I(ELXDLO101X)	CourseCode	DepartmentLevelOptional Course-II(EXCDLO202X)
ELXDLO1011	AdvancedProcessorArchitecture-I	ELXDLO2021	Advanced ProcessorArchitectu re-II
ELXDLO1012	NextGenerationArtificial IntelligenceandMachineLearning	ELXDLO2022	Cloud Computing
ELXDLO1013	MicroelectronicsDevices	ELXDLO2023	Nanoelectronics
ELXDLO1014	AdvancedDigitalImageProcessing	ELXDLO2024	DeepLearningandComputerV ision

SEMESTER–III

Course Code	CourseName	TeachingScheme(Hours)			CreditsAssigned			
		Theory	Practical	Tutorial	Theory	Practical	Tutorial	Total
ELXS3031	Seminar	---	06	---	---	03	---	03
ELXD3031	Dissertation-I	---	24	---	---	12	---	12
TOTAL		---	30	---	---	15	---	15

Course Code	CourseName	ExaminationScheme							
		TheoryMarks				Term Work	Practical	Oral	Total
		InternalAssessment			End Sem Exam				
		Test 1	Test 2	Average					
ELXS3031	Seminar	---	---	---	---	50	---	50	100
ELXD3031	Dissertation-I	---	---	---	---	100	---	---	100
TOTAL						150		50	200

SEMESTER–IV

Course Code	CourseName	TeachingScheme(Hours)			CreditsAssigned			
		Theory	Practical I	Tutorial	Theory	Practical	Tutorial	Total
ELXD4041	Dissertation-II	---	30	---	---	15	---	15
TOTAL		---	30	---	---	15	---	15

Course Code	CourseName	ExaminationScheme							
		TheoryMarks				Term Work	Practical	Oral	Total
		InternalAssessment			End Sem Exam				
		Test1	Test2	Average					
ELXD4041	Dissertation-II	---	---	---	---	100	---	100	200
TOTAL						100		100	200

Note:

- In case of Seminar (ELXS3031), 01 Hour / week / student should be considered for the calculation of load of a teacher
- In case of Dissertation I (ELXD3032) and Dissertation II (ETXD4041), 02 Hour/week/students should be considered for the calculation of load of a teacher

Course Code	Course Name	Teaching Scheme (Hours)			Credits Assigned			
		Theory	Practical	Tutorial	Theory	Practical	Tutorial	Total
ELXC1012	Advanced VLSI Design	03	---	---	03	---	---	03

Course Code	Course Name	ExaminationScheme							
		TheoryMarks				Term Work	Practical	Oral	Total
		InternalAssessment			End SemExam				
		Test 1	Test 2	Avg					
ELXC1012	Advanced VLSI Design	20	20	20	80	---	---	---	100

Course Pre-requisites:-

1. VLSI Design
2. IC Technology
3. Analog and Mixed Signal VLSI Design

Course Objectives:-

1. To make students understand & appreciate analytical approach for design of analog VLSI Design
2. To make students ready for design of coexistence of analog and digital circuit and the system level issues

Course Outcomes:-

1. Tackle with the system level issues for mixed VLSI design
2. Explain working of certain basic analog building blocks
3. Design different data converters
4. Implement and comment on performance of Memory devices.
5. State the significance of PLL in mixed VLSI design.

Module No.	Topics	Hrs.
01	Analog and discrete-time signal processing	03
	Mixed-Signal Layout Issues, Floor-planning, Power Supply and Grounding Issues, Guard Rings	
02	Analog integrated continuous-time and discrete-time filters	08
	MOSFETs as switches, Speed considerations, Precision Considerations, Charge injection cancellation, Unity gain buffer, Non-inverting amplifier and integrator, Analog multipliers, Loop Filters, Switched Capacitor filter	
03	Special-purpose CMOS circuits.	08
	Schmitt trigger, Multi-vibrator Circuits, Ring oscillators, VCO, Voltage Generators	
04	Data Converters	08
	Basics of Analog to digital converters (ADC) Basics of Digital to analog converters (DAC) DACs Successive approximation ADCs Dual slope ADCs High-speed ADCs (e.g. flash ADC, pipeline ADC and related architectures) High-resolution ADCs (e.g. delta-sigma converters)	
05	Memory	06
	ROM, EPROM, F-N model, RAM Memory structure Array Design, sensing and operation of memory cell.	
06	Phase Lock Loop	06
	Mixed-Signal layout Interconnects Phase locked loops Delay locked loops. Simple PLL, Charge pump PLL, Non ideal effects in PLL, Delay locked loops and applications of PLL in integrated circuits	
TOTAL		39

Reference Books:-

1. CMOS mixed-signal circuit design by R. Jacob Baker, Wiley India, IEEE press, reprint 2008.
2. Design of analog CMOS integrated circuits by Behzad Razavi, McGraw-Hill, 2003.
3. CMOS circuit design, layout and simulation by R. Jacob Baker, Revised second edition, IEEE press, 2008.
4. CMOS Integrated ADCs and DACs by Rudy V. de Plassche, Springer, Indian edition, 2005.
5. Electronic Filter Design Handbook by Arthur B. Williams, McGraw-Hill, 1981.
6. Design of analog filters by R. Schauman, Prentice-Hall 1990 (or newer additions)
7. An introduction to mixed-signal IC test and measurement by M. Burnset al., Oxford university press, first Indian edition, 2008.

ResearchPublication:-

1. Lanny L. Lewyn, Trond Ytterda, Carsten Wulff, and Kenneth Martin, "Analog circuit Design in Nanoscale Technologies", Proceedings of the IEEE Vol.97, No.10, October 2009
2. Chi-Sheng Lin, Bin-Da Liu, "A new successive approximation architecture for low-power low-cost CMOS A/D converter," IEEE Journal of Solid State Circuits, Vol.30, Issue. 1, Pages:54-62, 2003.

Internal Assessment(IA):

Two tests must be conducted which should cover at least 80% of the syllabus. The average marks of both the tests will be considered as final IA marks

End Semester Examination:

1. Question paper will comprise 6 questions, each of 20 marks.
2. Total 4 questions need to be solved.
3. Question No.1 will be compulsory and based on entire syllabus where in sub questions of 2 to 5 marks will be asked.
4. Remaining questions will be selected from all the modules

Course Code	Course Name	Teaching Scheme			Credits Assigned			
		Theory	Practical and Oral	Tutorial	Theory	TW/Practical and Oral	Tutorial	Total
ELXC1013	Power Electronics System Design	03	--	--	03	--	--	03

Subject Code	Subject Name	ExaminationScheme							
		TheoryMarks					Term Work	Practical andOral	Total
		Internalassessment			End Sem. Exam	Examdu rationH ours			
		Test 1	Test 2	Avg					
ELXC1013	PowerElec tronicsSyst em Design	20	20	20	80	3	--	--	100

Course Objectives:

1. To make the students understand and appreciate the analytical approach for design of power electronics systems.
2. To make the students ready for research & development oriented jobs in academia and industry by introducing recent research advancements in power electronic converters and their applications in distributed generation and smart grids.

Course Outcomes:

After successful completion of the course students will be able to:

1. **Understand** power semiconductor device structures for adjustable speed motor control applications.
2. **Apply** the concepts of mathematical modelling and computer simulation to power electronics systems.
3. **Design** the new topologies of DC-AC inverters like multi-level and 4-leg inverters.
4. **Interpret** various issues involved in the parallel operation of inverters as a part of distributed generation system.
5. **Select** appropriate three phase AC voltage controllers depending on the application.
6. **Analyze** vital role played by power electronic converters in distributed generation and smart grids.

Note: The action verbs according to Bloom's taxonomy are highlighted in bold.

Module No.	Unit No.	Contents	Hrs.
1		Analysis of Power Devices	05
	1.1	Power MOSFET, SCR, IGBT, selection criteria for switching devices	
	1.2	EMI-EMC issues, protection circuits: Antisaturation protection for IGBT and power MOSFET, overload protection, thermal protection.	
2		Simulation of Power Electronic Converters and Systems	6
	2.1	Introduction to circuit oriented simulators like SPICE, MATLAB, SCILAB, comparison of these simulators	
	2.2	Study of transformations from 3-phase to stationary reference frame (Clark transform) and rotating reference frame, decoupled closed-loop control strategies for converters based on these transformations.	
3		Modelling and Control of Power Electronic Systems	08
	3.1	Concept of zero-order hold (ZOH), first-order hold (FOH) and second-order hold (SOH) elements, energy factor, models of AC-DC, DC-AC, AC-AC and DC-DC converters as simple ZOH, FOH and SOH	
	3.2	PI control for AC-DC converters, PI control for DC-AC converters and AC-AC (AC-DC-AC) converters, PID control for DC-DC converters, closed-loop stability analysis.	
4		Inverters (DC-AC Converters)	10
	4.1	Multilevel inverter topologies and switching, introduction to 4-leg inverters (basic working without SVM techniques)	
	4.2	Study of inverter topologies: online, line-interactive, stand-by, methods of parallel operation of inverters: droop, and master & slave control.	
5	5.1	Three phase AC Voltage Controllers	4
		Three-phase full wave controller with R, RL-load, Input power factor, static switches.	
6		Grid Interface of Renewable Energy Sources	6
	6.1	Inverter interfacing control strategies for transferring wind and solar energy to grid, synchronization with grid using phase-locked loop	
	6.2	Concept of distributed generation systems, microgrids, smart grids.	
Total			39

TextBooks:

1. N.Mohan, T.M.Undeland, W.P.Robbins, Power Electronics: Converters Application and Design, John Wiley & Sons, USA, 2003.
2. M. H. Rashid, Power Electronics: Circuits, Devices, and Applications, Pearson Education India, 2009.
3. R.W.Erickson, D.Maksimovic, Fundamentals of Power Electronics, Springer USA, 2001.
4. F. L. Luo, H. Ye, M. H. Rashid, Digital Power Electronics and Applications, Elsevier Academic Press, USA, 2005.
5. H. Akagi, E. H. Watanabe, M. Aredes, Instantaneous Power Theory and Applications to Power Conditioning, IEEE Press/John Wiley & Sons Ltd., USA, 2007.
6. B.K.Bose, Modern power electronics and AC drives, Prentice Hall PTR, 2002.

Reference Books/Research papers:

1. Q.-C. Zhong, T. Hornik, Control of Power Inverters in Renewable Energy And Smart Grid Integration, IEEE Press/John Wiley & Sons, Ltd., USA, 2013.
2. J.-S. Lai and F. Z. Peng, Multilevel converters – A new breed of power converters, IEEE Transactions on Industry Applications, vol.32, no.3, pp.509-517, May/Jun 1996. URL: <http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=502161&number=10824>
3. T.Kawabata and S.Higashino, Parallel operation of voltage source inverters, IEEE Transactions on Industry Applications, vol. 24, no. 2, pp. 281–287, 1988.
URL:
<http://ieeexplore.ieee.org/xpl/login.jsp?tp=&arnumber=2868&url=http%3A%2F%2Fieeexplore.ieee.org%2Fiel1%2F28%2F164%2F00002868>
4. W. C. Lee, T. K. Lee, S. H. Lee, K. H. Kim, D. S. Hyun, and I. Y. Suh, A master and slave control strategy for parallel operation of three-phase UPS systems with different ratings, Proceedings of the 19th Annual IEEE Applied Power Electronics Conference & Exposition, (Anaheim, California, USA), pp. 456–462, Feb. 2004.
URL:
<http://ieeexplore.ieee.org/xpl/login.jsp?tp=&arnumber=1295848&url=http%3A%2F%2Fieeexplore.ieee.org%2Fiel5%2F9082%2F28818%2F01295848.pdf%3Farnumber%3D1295848>

Internal Assessment (IA):

Two tests must be conducted which should cover at least 80% of syllabus. The average marks of both the tests will be considered as final IA marks.

End Semester Examination:

1. Question paper will consist of 6 questions, each of 20 marks.
2. Total 4 questions need to be solved.
3. Question No. 1 will be compulsory and based on entire syllabus where in sub Questions of 2 to 5 marks will be asked.
4. Remaining questions will be selected from all the modules

CourseCode	CourseName	Teaching Scheme(Hours)			Credits Assigned			
		Theory	Practical	Tutorial	Theory	Practical	Tutorial	Total
ELXDLO1013	MicroelectronicsDevices	04	---	---	04	---	---	04

Course Code	CourseName	ExaminationScheme							
		Theory Marks				Term Work	Practical	Oral	Total
		InternalAssessment			End SemExam				
		Test 1	Test 2	Average					
ELXDLO1013	Microelectronics Devices	20	20	20	80	---	---	---	100

CoursePre-requisites:-

- Electronicdevices:OperationandCharacteristics

CourseObjectives:-

- Tolearn &applybasic conceptsof semiconductorphysicsrelevanttoelectronicdevices
- Toanalyze&explainoperationofsemiconductordevicesintermsoftheirphysicalstructure
- Toestimatevarious deviceparameters &theirmeasurement
- Todescribe&usethedevic& circuitmodelsof semiconductordevicesof varyinglevelofcomplexity

CourseOutcomes:-

- Abilitytoapply&explainbasic semiconductor conceptsapplicable tothedevices
- Abilityto describetheunderlyingphysics&principles of operation ofvariousdevices
- Abilitytcreate&applylinearincrementalequivalentcircuitmodelsforBJT&MOSFET
- Ability to determine parameter values for large signal & incremental linear equivalentcircuit models for the p-n diodes, BJT & MOSFET based on knowledge of devicestructure,dimensions & bias conditions

Module No.	Unit No.	Topics	Hrs.
1	Basic Semiconductor Physics		08
	1.1	Review of quantum mechanics,	
	1.2	Electrons in periodic lattices, E _k diagrams, Quasi-particles in semiconductors, electrons, holes and phonons	
	1.3	Boltzmann transport equation and solution in the presence of low electric and magnetic fields-mobility and diffusivity	
2	Semiconductor Junction		08
	2.1	p-n junction action, Abrupt junction, Linearly graded junction, Static I-V Characteristic of p-n junction, Electrical breakdown in p-n junctions	
	2.2	Dynamic behaviour of p-n junction diode	
	2.3	Majority carrier diodes	
	2.4	Schottky, homo- and hetero-junction band diagrams and I-V characteristics	
3	Modeling Bipolar Device Phenomena		05
	3.1	Injection and Transport Model	
	3.2	Continuity Equation	
	3.3	Transistor Models: Ebers-Moll and Gummel-Poon Model	
	3.4	SPICE modeling, temperature and area effects	
4	MOSFET Modeling		08
	4.1	Introduction, Inversion Layer,	
	4.2	Threshold Voltage	
	4.3	Gradual Channel Approximation, MOS Transistor Current	
	4.4	Temperature, Short channel and Narrow Width Effect	
	4.5	Characterization of MOS capacitors: HF and LF CVs	
	4.6	Models for Enhancement, Depletion Type MOSFET	
5	Modeling of Hetero Junction Devices		06
	5.1	Bandgap Engineering	
	5.2	Band gap Offset at abrupt Hetero-junction	
	5.3	Modified current continuity equations	
	5.4	Hetero Junction bipolar transistors (HBTs), Si-Ge	
6	Monte Carlo Particle Modeling of Semiconductor Devices		04
	6.1	The Monte Carlo method	
	6.2	Application of Monte Carlo techniques to device modeling	
TOTAL			39

ReferenceBooks:-

1. M.S.Tyagi, "IntroductiontoSemiconductorMaterialsandDevice", JohnWiley&sons, 1991
2. BenG.Streetman&S.K.Bannerjee, "SolidStateElectronicDevices" 6thedition, PrenticeHall
3. RichardS.Muller&TheodoreI.Kummins, "DeviceElectronicsforIntegratedCircuits", JohnWiley& Sons, 2nd edition (1986)
4. A.S.Grove, "Physics&TechnologyforSemiconductorDevices", McGrawHill, 3rdedition (2007)
5. DonaldA.Neamen, "SemiconductorDevices&Physics", McGrawHill, 3rdedition(2007)
6. M.H.Rashid, "SPICEforCircuits&Electronics", PrenticeHall(1995)
7. A.Vladimirescu, "TheSPICE Book", JohnWiley&Sons, NewYork(1994)

ResearchPublications:-

1. ChristopherM.Snowden, "SemiconductorDeviceModeling" Rep.Prog.Phys. Vol.48, pp.223-275
2. C.Moglestue,,,"MonteCarloparticlemodelingofsmallsemiconductordevices" Computer Methods in Applied Mechanics & Engineering Vol. 30 (1982) pp. 173-208; North-Holland Publishing

InternalAssessment(IA):

Two tests must be conducted which should cover at least 80% of the syllabus. The average marks of both the test will be considered as final IA marks

EndSemesterExamination:

1. Question paper will comprise 6 questions, each of 20 marks.
2. Total 4 questions need to be solved.
3. Question No.1 will be compulsory and based on entire syllabus wherein sub questions of 2 to 5 marks will be asked.
4. Remaining questions will be selected from all the modules

Subject Code	Subject Name	Teaching Scheme			Credits Assigned			
		Theory	Practical	Tutorial	Theory	Practical	Tutorial	Total
ELXL1011	Power Electronics System Design Lab	--	02	--	--	01	--	01

Subject Code	Subject Name	ExaminationScheme							
		Theory Marks					Term Work	Practical AndOral	Total
		Internalassessment			End Sem. Exam	Examdu rationH ours			
		Test 1	Test 2	Avg ofTest 1and Test 2					
ELXL1011	PowerElect ronicsSyste m DesignLab	-	-	-	-	-	25	25	50

Term Work:

At least 10 experiments covering the entire syllabus of ELXC1013 (**Power Electronics System Design**) should be set to have well predefined inference and conclusion. The experiments should be student centric and attempt should be made to make experiments more meaningful, interesting. Simulation experiments are also encouraged. Experiments must be graded from time to time. The grades should be converted into marks as per the Credit and Grading System manual and should be added and averaged. The grading and term work assessment should be done based on this scheme. The final certification and acceptance of term work ensures satisfactory performance of laboratory work and minimum passing marks in term work. Practical and Oral exams will be based on the entire syllabus.

Laboratory Outcomes:

After successful completion of the course students will be able to:

1. **Analyze** selection criteria for power switching devices.
2. **Simulate** the power converters using simulation software like MATLAB, SCILAB and PSPICE.
3. **Design** and simulate closed loop control system for power converters.
4. **Simulate** a three phase power converters.
5. **Understand** the application of power electronic system.

Note: The action verbs according to Bloom's taxonomy are highlighted in bold.

Suggested List of Experiments

Sr. No.	Experiment Title
1	To study selection criteria for power switching devices.
2	To study PSpice as circuit oriented simulator for power converters.
3	To study MATLAB as circuit oriented simulator for power converters.
4	To study SCILAB as circuit oriented simulator for power converters.
5	To study ZOH, FOH and SOH model of power converters.
6	To study PI and PID control of power converters.
7	To study three phase inverter with R, RL load.
8	To study multilevel inverter topologies.
9	To study three phase controlled rectifier with R/RL load.
10	To study grid interface of renewable energy sources.

Note: Experiments can be performed online using simulation software as well as hardware. Free simulation software SCILAB can be used to perform the experiments.

(Expected percentage of H/w and software experiments should be 60% & 40% respectively)

Note:

Suggested List of Experiments is indicative. However, flexibility lies with individual course instructors to design and introduce new, innovative and challenging experiments, (limited to maximum 30% variation to the suggested list) from within the curriculum, so that the fundamentals and applications can be explored to give greater clarity to the students and they can be motivated to think differently.

Course Code	CourseName	TeachingScheme(Hrs)			Credits Assigned			
		Theory	Practical	Tutorial	Theory	Practical	Tutorial	Total
ELXC203	Advanced Digital Signal Processing	3	-	-	4	-	-	4

Course Code	Course Name	ExaminationScheme							
		Theory Marks							
		Internalassessment			EndSem. Exam	Term Work	Practical	Oral	Total
		Test 1	Test 2	Avg. Of Test 1 & Test 2					
ELXC203	Advanced Digital Signal Processing	20	20	20	80	-	-	-	100

CoursePre-requisites:

SignalsandSystems,DigitalSignalProcessing,ProbabilityandRandomprocesses.

CourseObjectives:

1. To understand DSP techniques in different fields of modern day applications.
2. To study multirate DSP algorithms and filter bank analysis for real world applications.
3. To develop a solid foundation in linear prediction analysis and optimum filtering concepts.
4. To learn thoroughly LMS and RLS algorithms which are at the heart of the adaptive systems.
5. To gain deep insight into spectrum estimation algorithms.

CourseOutcomes:

Students will be able to

1. Apply multirate processing techniques in practical applications.
2. Design optimum filters suited for different applications.
3. Design and simulate adaptive systems.
4. Extract information from spectral analysis of signals.
5. Design and test signal processing algorithms for various tasks.

Module No.	Unit No	Topics	Hrs
01		Introduction and Review	04
	1.1	Basic DSP examples in block diagrams, Typical DSP in real world applications.	02
	1.2	Review of FIR & IIR filters, Sampling and Reconstruction of signals, Analog to digital and Digital to analog conversions.	02
02		Multirate Digital Signal Processing	12
	2.1	Introduction, Decimation by a factor D, Interpolation by a factor I, Sampling rate conversion by a rational factor I/D.	03
	2.2	Implementation of sampling rate conversion, Multistage implementation of sampling rate conversion.	03
	2.3	Sampling rate conversion of band pass signal, sampling rate conversion by arbitrary factor, Applications of multirate signal processing.	03
	2.4	Digital filter banks, Two channel Quadrature Mirror filter banks.	03
03		Linear Prediction and Optimum filters	07
	3.1	Random signals, Correlation functions, Power Spectra, Innovations representation of a Stationary random Process	03
	3.2	Forward and Backward Linear predictions.	02
	3.3	Solution of Normal equations. The Levinson-Durbin Algorithm.	02
04		Adaptive Digital Filters	06
	4.1	FIR adaptive filters. Steepest descent adaptive filter, LMS algorithms, Normalized LMS, Application in noise cancellation.	04
	4.2	Adaptive Recursive filters.	02
05		Power Spectrum Estimation	06
	5.1	Estimation of spectra from finite duration observations of signals.	02
	5.2	Nonparametric methods for power spectrum estimation.	02
	5.3	Parametric methods for power spectrum estimation.	02
06		Applications of DSP	04
	6.1	Biomedical applications, ECG signal analysis, QRS template, QRS detection methods etc.	02
	6.2	Speech processing applications, Wideband and narrowband spectrograms.	02
		Total	39

ReferenceBooks:

1. DigitalSignal ProcessingPrinciples ,algorithms and applications ,John. G. Proakis ,D.G.Manolakis. 4/e,Pearson.
2. DigitalSignalProcessing,APracticalapproach.Emmanuel.C.IfeachorB.W.Jervis.Pearson.
3. DigitalSignalProcessing.Acomputerbasedapproach,S.K.Mitra,TataMcGrawHill.
4. StatisticalDigitalSignalProcessing,Monson.H.HAYES,WileyIndia.
5. IntroductiontoDigitalSpeechProcessing, L.RRabiner&R.W Schafer, Pearson.
6. DiscretetimeSignalsProcessing,Oppenheim &Schaffer,Pearson.

RecommendedResearchPapersforReading:

1. **P.Vaidyanathan**(1990). "*Multirate Digitalfilters,Filterbanks,Polyphasenetworkand applications: Atutorial*" Proc.IEEE vol 78,No 1,pp 56-90.
2. **SchoederM.R**(1985) "*Linearpredictivecodingofspeech:Reviewandcurrentdirections*"IEEECommun. Magvol 23 , pp 54-61
3. **Widrow.B**(1975) "*Adaptivenoisecancelling,PrinciplesandApplications*"ProcIEEE,vol 63, pp 1692-1716
4. **WidrowB**(1976) "*StationaryandNonstationary characteristicsoftheLMSadaptivefilter*"Proc IEEE ,vol 64,pp 1151-1162
5. **ThomsonD.J**(1969) "*Spectralestimation&Harmonicanalysis*"ProcIEEEvol70, pp1055-1096

InternalAssessment(IA):

Two tests must be conducted which should cover at least 80% of the syllabus. The average marks ofboththetestwillbe consideredasfinalIAMarks

EndSemesterExamination:

1. Questionpaperwill comprise6questions,eachof20marks.
2. Total4questionsneedtobesolved.
3. Question No.1 will be compulsory and based on entire syllabus wherein sub questions of 2 to5marks willbeasked.
4. Remainingquestionswill beselectedfromall themodules

Course Code	CourseName	TeachingScheme(Hrs)			Credits Assigned			
		Theory	Practical	Tutorial	Theory	Practical	Tutorial	Total
ELXL204	LAB-1V AdvancedDigital SignalProcessingLAB	-	2	-	-	1	-	1

Course Code	Course Name	ExaminationScheme							
		Theory Marks				Term Work	Practical	Oral	Total
		Internalassessment			EndSem.E xam				
		Test 1	Test 2	Avg. OfTest1& Test 2					
ELXL204	LAB-1V AdvancedDigital signalProcessingLAB	-	-	-	-	25	-	25	50

CoursePre-Requisites:

1. Basic knowledge of Signals and Systems, DSP.
2. Acquaintance of Simulation languages and software tools.

CourseObjectives:

1. To design and simulate basic DSP systems and multirate systems for practical applications.
2. To design and simulate DSP systems for spectral analysis of signals and optimum filters for different applications
3. To design and simulate adaptive filters for real world applications

CourseOutcomes:

Students will be able to

1. Implement basic DSP algorithms and multirate techniques for various situations.
2. Implement optimum filters for real world applications and extract spectral information.
3. Design and test adaptive filter systems for practical applications.

List of Experiments:

1. Basic filtering operations, like noise reduction using FIR filter, enhancement of ECG signal using notch filtering etc.
2. IIR filter. Simulation of Digital audio equalizer.
3. Biomedical signal processing, ECG signal processing.
4. Algorithms in DTMF tone generation.
5. Oversampling and Analog to digital conversion resolution.
6. Sampling rate reduction by an integer factor, sampling rate increase by an integer factor.
7. Changing Sampling rate by a non integer factor L/M .
8. Upsampling and Interpolation filter processes in CD audio systems.
9. Noise cancellation using adaptive filters.
10. System modeling using adaptive filters.
11. Line enhancement using linear prediction.
12. Subband decomposition and two channel perfect reconstruction QMF bank.

Students are required to perform any **six experiments** from the above list covering most of the topics in Advanced Signal processing and perform **one mini project** preferably based on any of the above topics 2, 4, 8, or 12.

Reference Books:

1. Digital Signal Processing Fundamentals & Applications. 2/e Li Tan & Jean Jiang Elsevier, Academic press.
2. Digital Signal Processing. A computer based approach, S.K. Mitra, Tata McGraw Hill.

SEMESTER III

CourseCode	CourseName	Credits
ELXS3031	Seminar	03

Guidelines for Seminar

- Seminar should be based on thrust areas in Electronics and Telecommunication Engineering
- Students should do literature survey and identify the topic of seminar and finalize in consultation with Guide/Supervisor.
- Students should use multiple literatures and understand the topic and compile the report in standard format and present in front of Panel of Examiners appointed by the Head of the Department/Institute of respective Programme.

Seminar should be assessed based on following points

- Quality of Literature survey and Novelty in the topic
- Relevance to the specialization
- Understanding of the topic
- Quality of Written and Oral Presentation

IMPORTANT NOTE:

1. Assessment of Seminar will be carried out by a pair of Internal and External examiner. The external examiners should be selected from approved panel of examiners for Seminar by University of Mumbai, OR faculty from Premier Educational Institutions / Research Organizations such as IIT, NIT, BARC, TIFR, DRDO, etc. OR a person having minimum Post-Graduate qualification with at least five years' experience in Industries.
2. Literature survey in case of seminar is based on the broader area of interest in recent developments and for dissertation it should be focused mainly on identified problem.
3. At least 4-5 hours of course on Research Methodology should be conducted which includes Literature Survey, Problems Identification, Analysis and Interpretation of Results and Technical Paper Writing in the beginning of 3rd Semester.

SEMESTER III

CourseCode	CourseName	Credits
ELXD3031/ELXD4041	Dissertation I/ Dissertation-II	12+15

Guidelines for Dissertation

- Students should do literature survey and identify the problem for Dissertation and finalize in consultation with Guide/Supervisor. Students should use multiple literature and understand the problem. Students should attempt solution to the problem by analytical/simulation/experimental methods. The solution to be validated with proper justification and compile the report in standard format.

Guidelines for Assessment of Dissertation I

- Dissertation I should be assessed based on following points
- Quality of Literature survey and Novelty in the problem
- Clarity of Problem definition and Feasibility of problem solution
- Relevance to the specialization
- Clarity of objective and scope
- Dissertation I should be assessed through a presentation by a panel of Internal examiners appointed by the Head of the Department/Institute of respective Programme.

Guidelines for Assessment of Dissertation II

- Dissertation II should be assessed based on following points
- Quality of Literature survey and Novelty in the problem
- Clarity of Problem definition and Feasibility of problem solution
- Relevance to the specialization or current Research/Industrial trends
- Clarity of objective and scope
- Quality of work attempted
- Validation of results
- Quality of Written and Oral Presentation
- Dissertation II should be assessed through a presentation jointly by Internal and External Examiners appointed by the University of Mumbai
- Students should publish at least one paper based on the work in reputed International/National Conference (desirably in Refereed Journal)